TO BEGIN WITH ALTERA FPGA KIT

EEP 201, Department of Electrical Engineering, IIT Delhi

1.CIRCUIT DESIGN

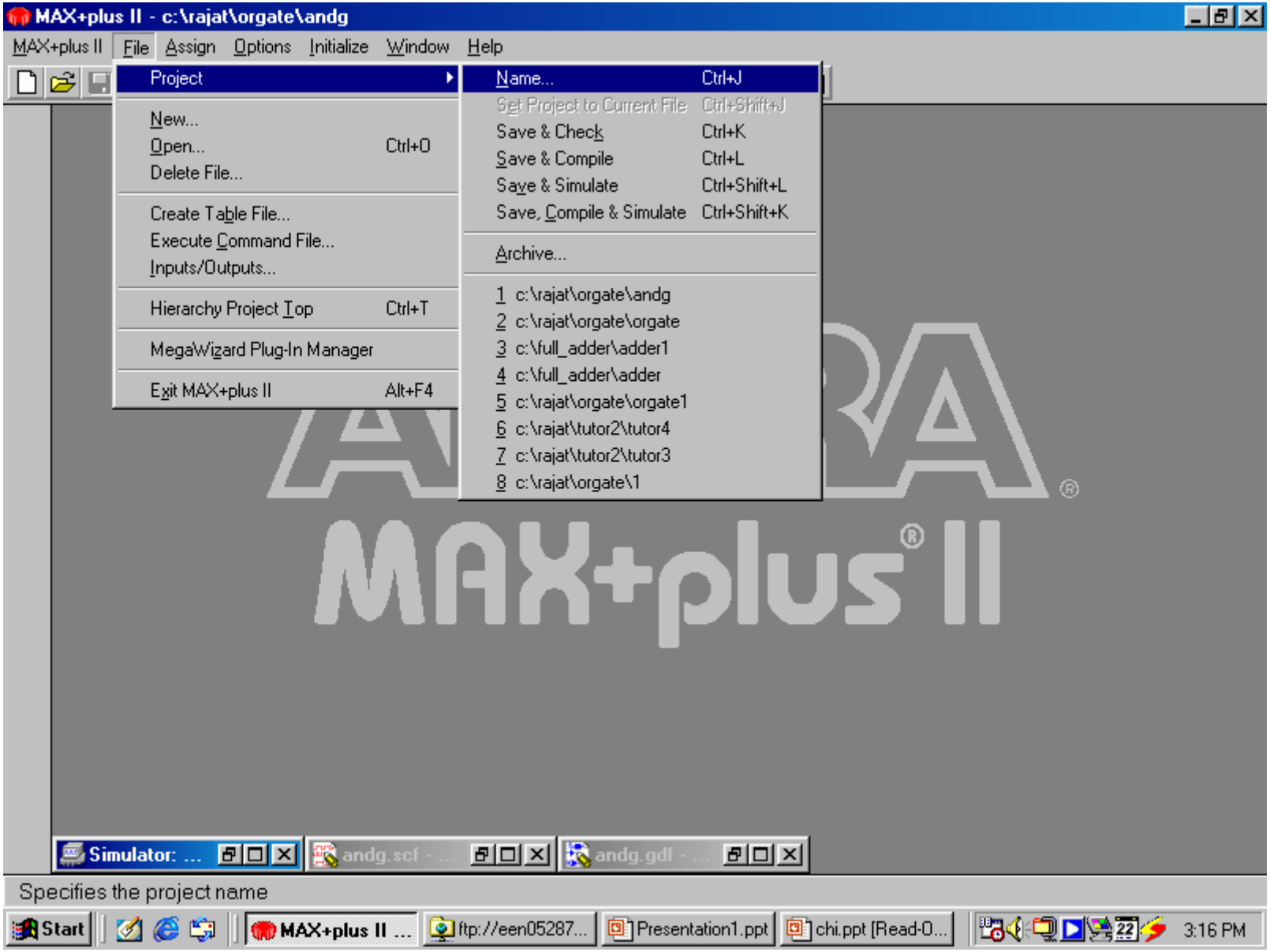
2.CIRCUIT SIMULATION

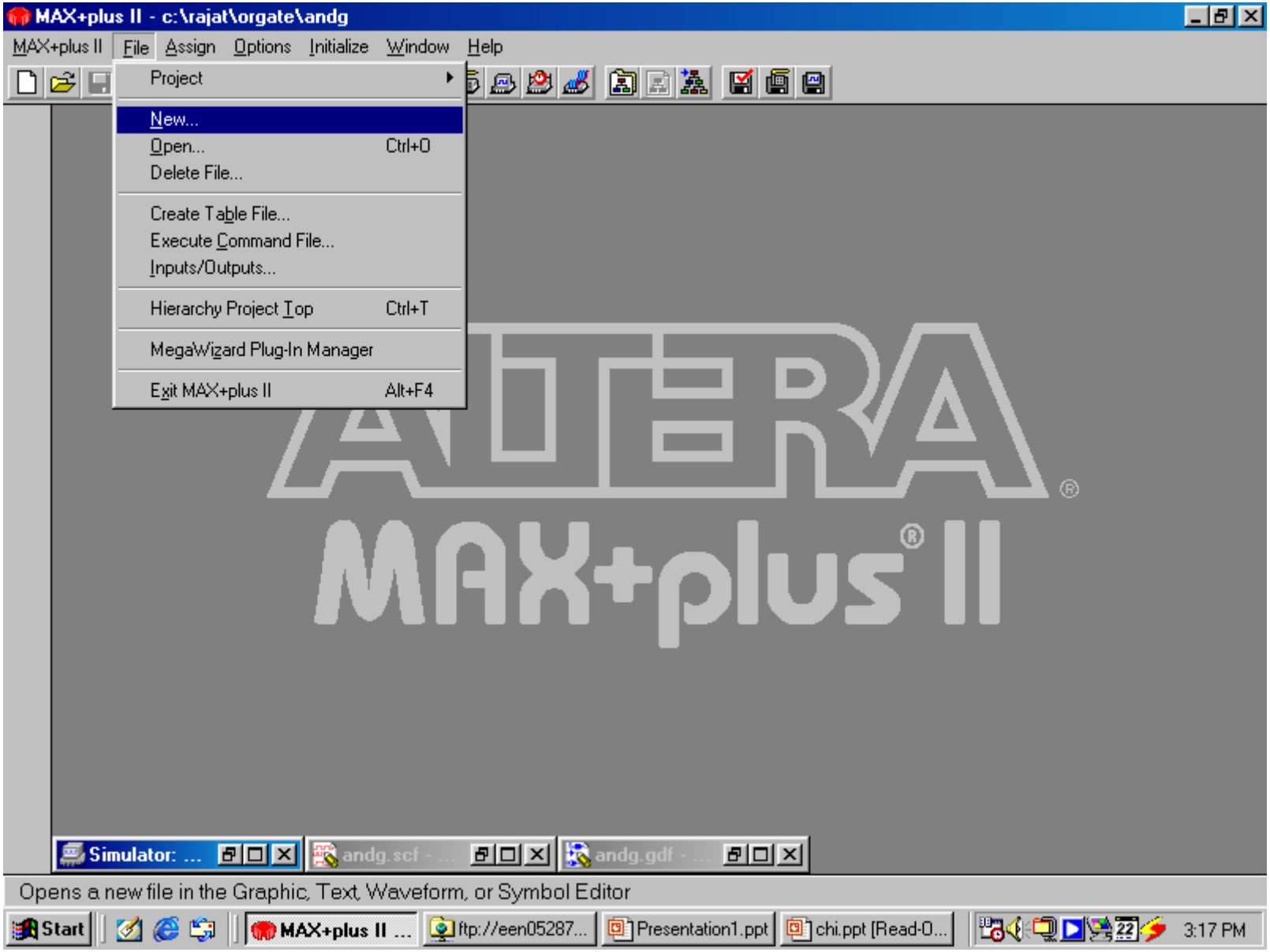
3.PROGRAMMING FPGA

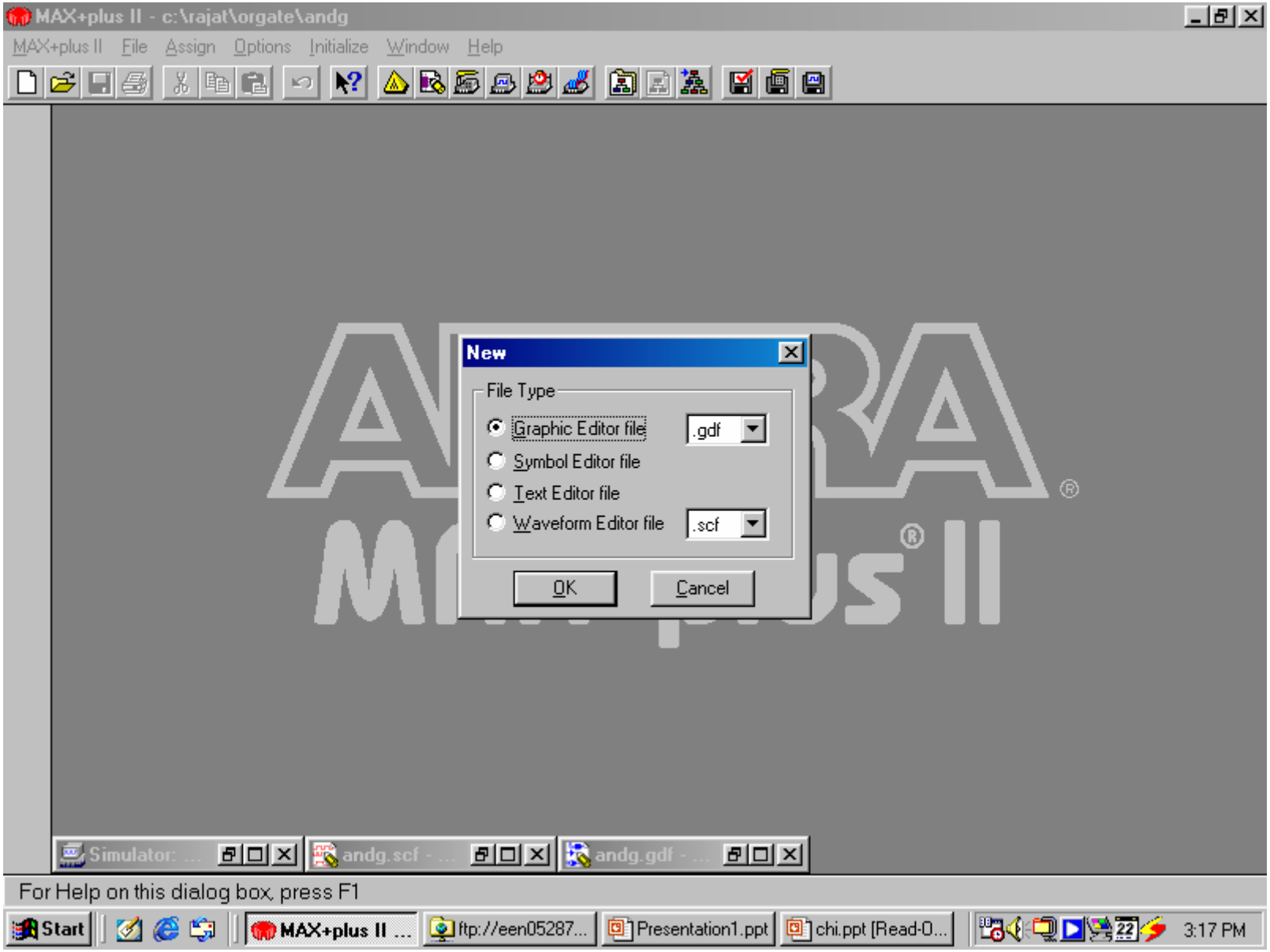
I. Circuit Design

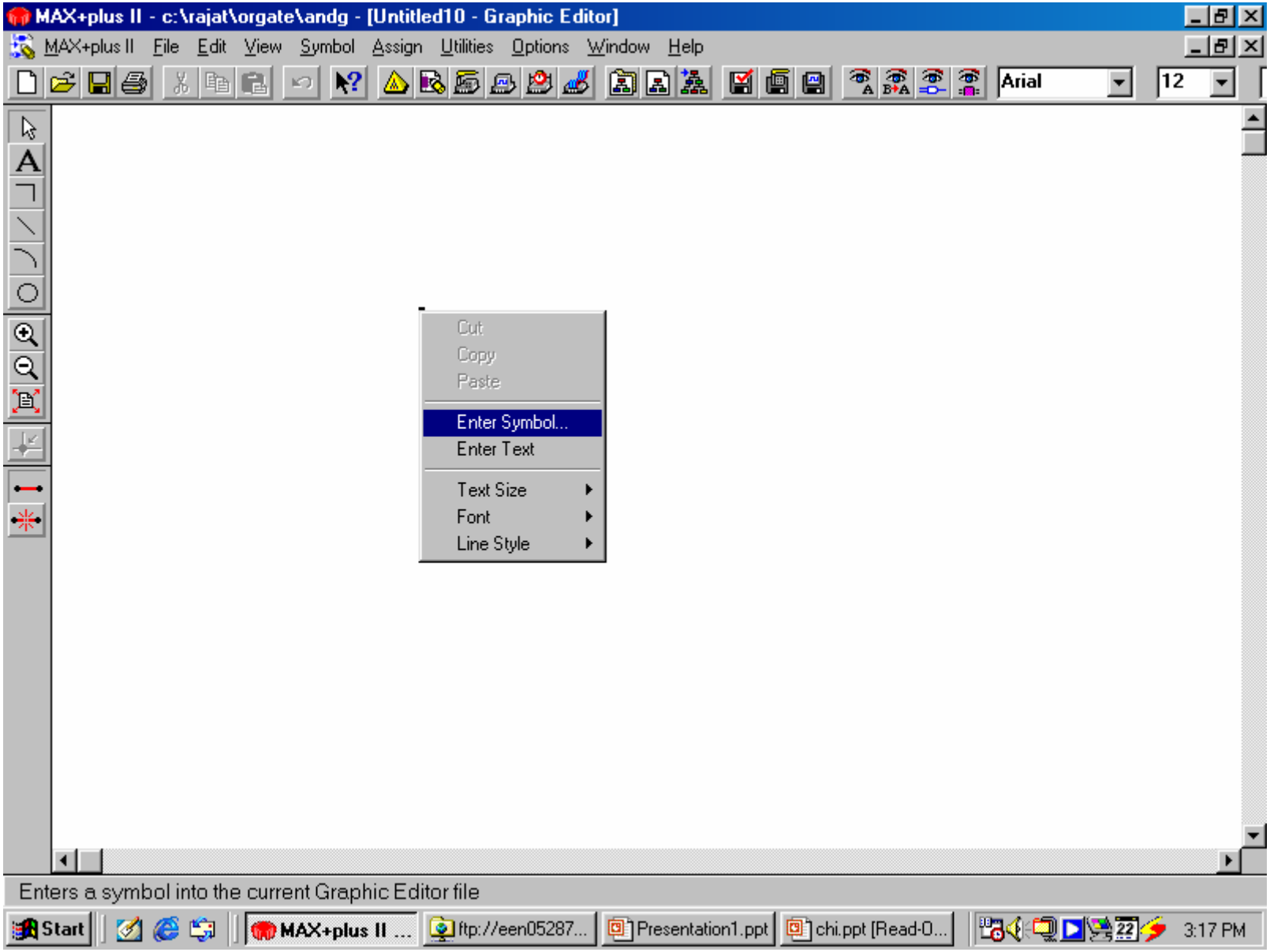
A. *New Design Creation*

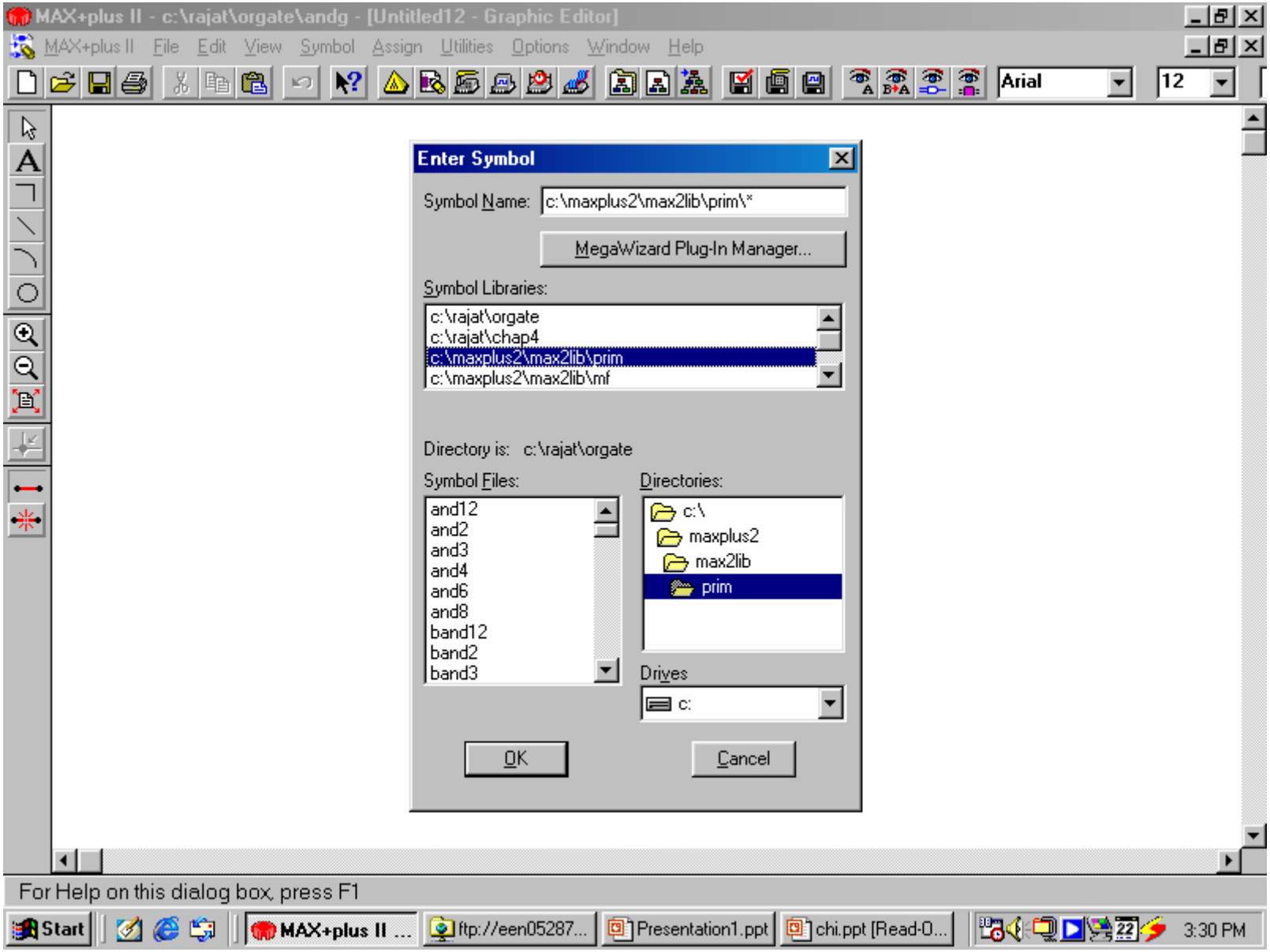
B. *Component Selection Process*


MAX+plus II - c:\rajat\orgate\andg
MAX+plus II
File
Assign
Options
Initialize
Window
Help
Project
New...
Open... Ctrl+O
Delete File...
Create Table File...
Execute Command File...
Inputs/Outputs...
Hierarchy Project Top Ctrl+T
MegaWizard Plug-In Manager
Exit MAX+plus II Alt+F4
Name... Ctrl+J
Set Project to Current File Ctrl+Shift+J
Save & Check Ctrl+K
Save & Compile Ctrl+L
Save & Simulate Ctrl+Shift+L
Save, Compile & Simulate Ctrl+Shift+K
Archive...
1 c:\rajat\orgate\andg
2 c:\rajat\orgate\orgate
3 c:\full_adder\adder1
4 c:\full_adder\adder
5 c:\rajat\orgate\orgate1
6 c:\rajat\tutor2\tutor4
7 c:\rajat\tutor2\tutor3
8 c:\rajat\orgate\1
MAX+plus II
Simulator: ...
andg.scf - ...
andg.gdf - ...
Specifies the project name
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:16 PM


MAX+plus II - c:\rajat\orgate\andg
MAX+plus II
File
Assign
Options
Initialize
Window
Help
Project
New...
Open... Ctrl+O
Delete File...
Create Table File...
Execute Command File...
Inputs/Outputs...
Hierarchy Project Top Ctrl+T
MegaWizard Plug-In Manager
Exit MAX+plus II Alt+F4
ALTERA
MAX+plus II
Simulator: ...
andg.scf - ...
andg.gdf - ...
Opens a new file in the Graphic, Text, Waveform, or Symbol Editor
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:17 PM


MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Assign Options Initialize Window Help
New
File Type
Graphic Editor file
.gdf
Symbol Editor file
Text Editor file
Waveform Editor file
.scf
OK
Cancel
Simulator: ...
andg.scf - ...
andg.gdf - ...
For Help on this dialog box, press F1
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:17 PM

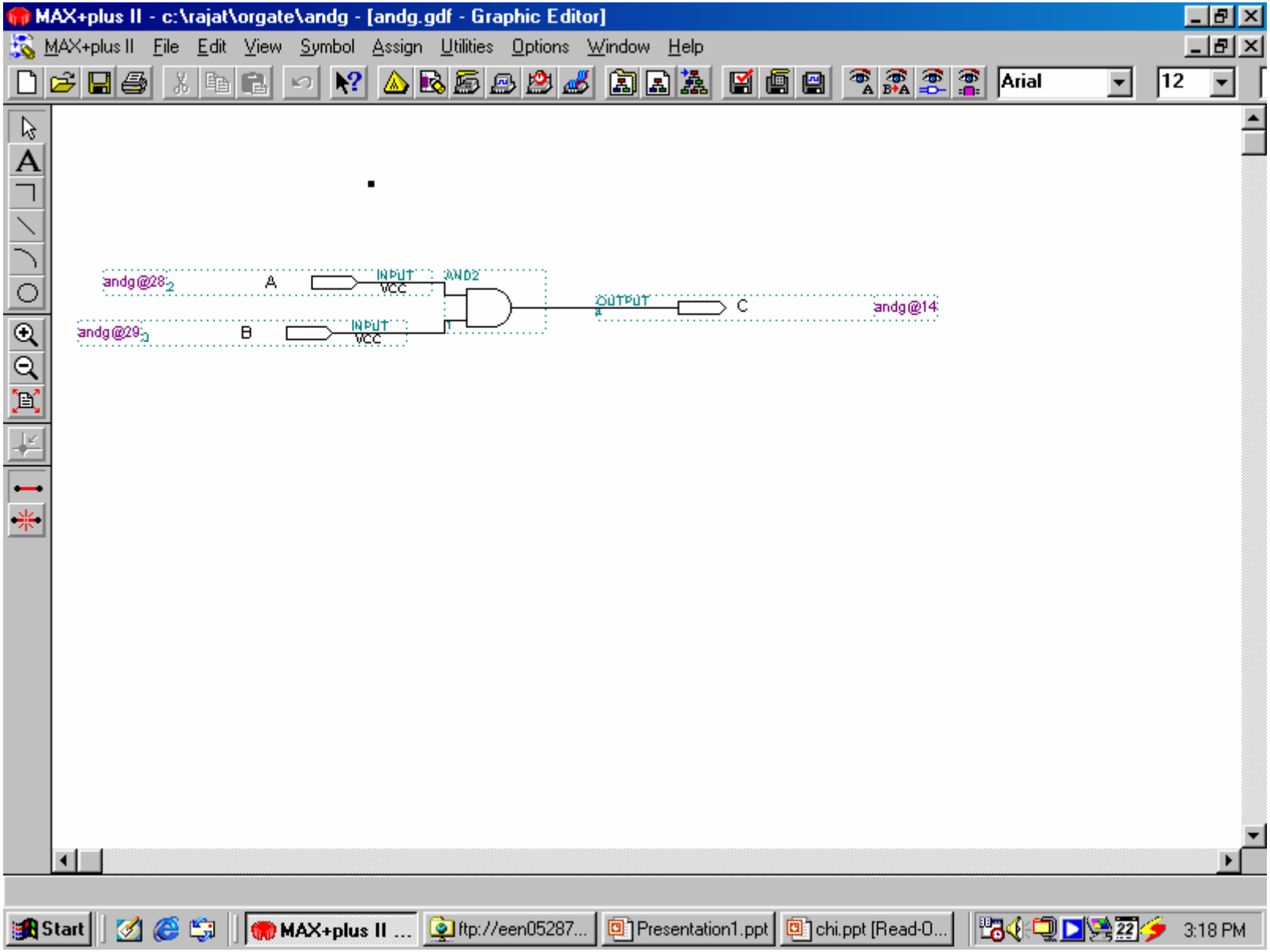

MAX+plus II - c:\rajat\orgate\andg - [Untitled10 - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Arial
12
Cut
Copy
Paste
Enter Symbol...
Enter Text
Text Size
Font
Line Style
Enters a symbol into the current Graphic Editor file
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:17 PM


MAX+plus II - c:\rajat\orgate\andg - [Untitled12 - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Arial
12
Enter Symbol
Symbol Name: c:\maxplus2\max2lib\prim*
MegaWizard Plug-In Manager...
Symbol Libraries:
c:\rajat\orgate
c:\rajat\chap4
c:\maxplus2\max2lib\prim
c:\maxplus2\max2lib\mf
Directory is: c:\rajat\orgate
Symbol Files:
and12
and2
and3
and4
and6
and8
band12
band2
band3
Directories:
c:\
maxplus2
max2lib
prim
Drives
c:
OK
Cancel
For Help on this dialog box, press F1
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:30 PM

I. Circuit Design

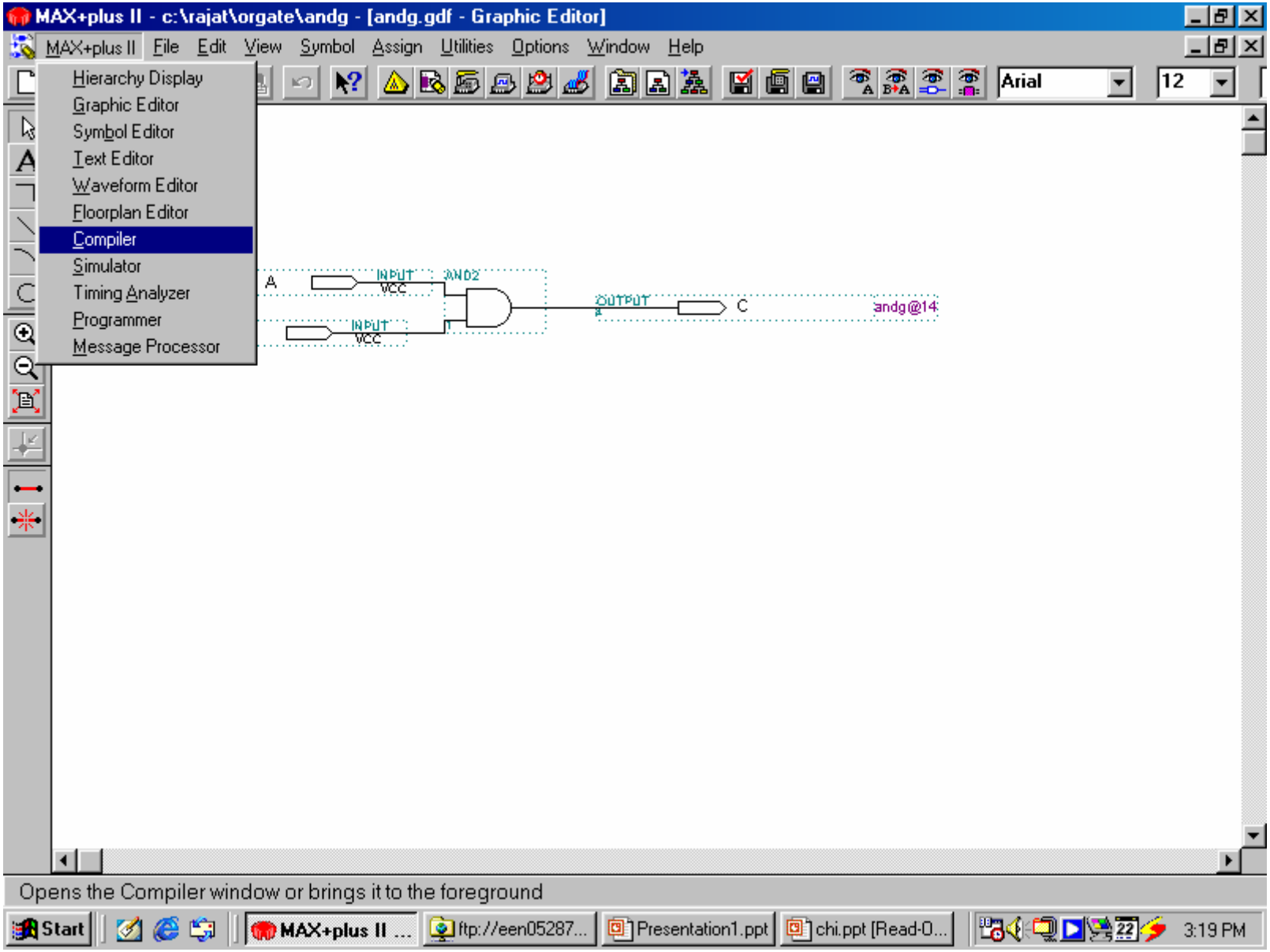
C. *Adding/Deleting Wires & Moving Components*

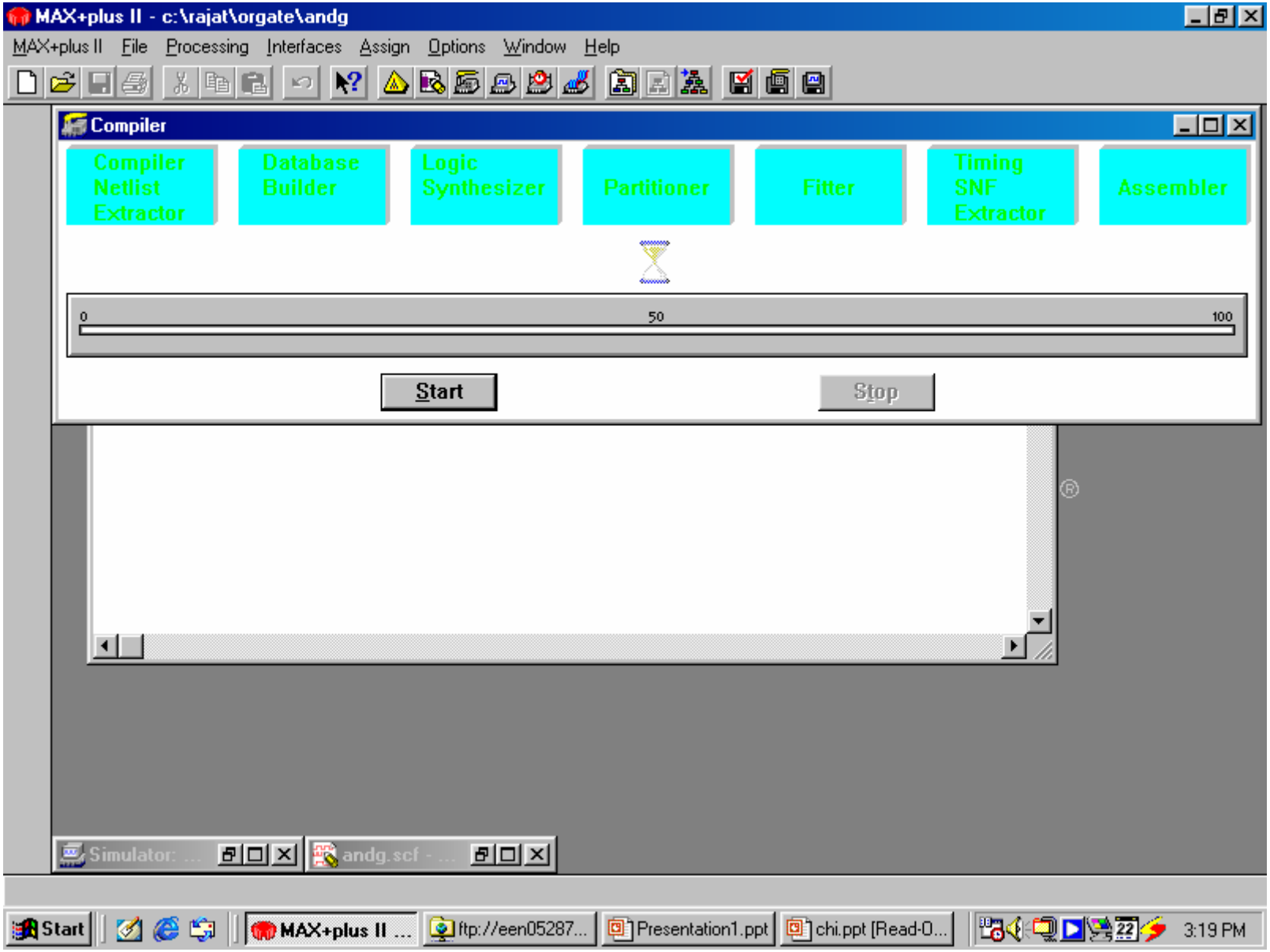
D. *Adding Input & Output Ports*


MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Arial
12
andg@28
A
INPUT
VCC
AND2
andg@29
B
INPUT
VCC
OUTPUT
C
andg@14
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:18 PM

II. Circuit Simulation

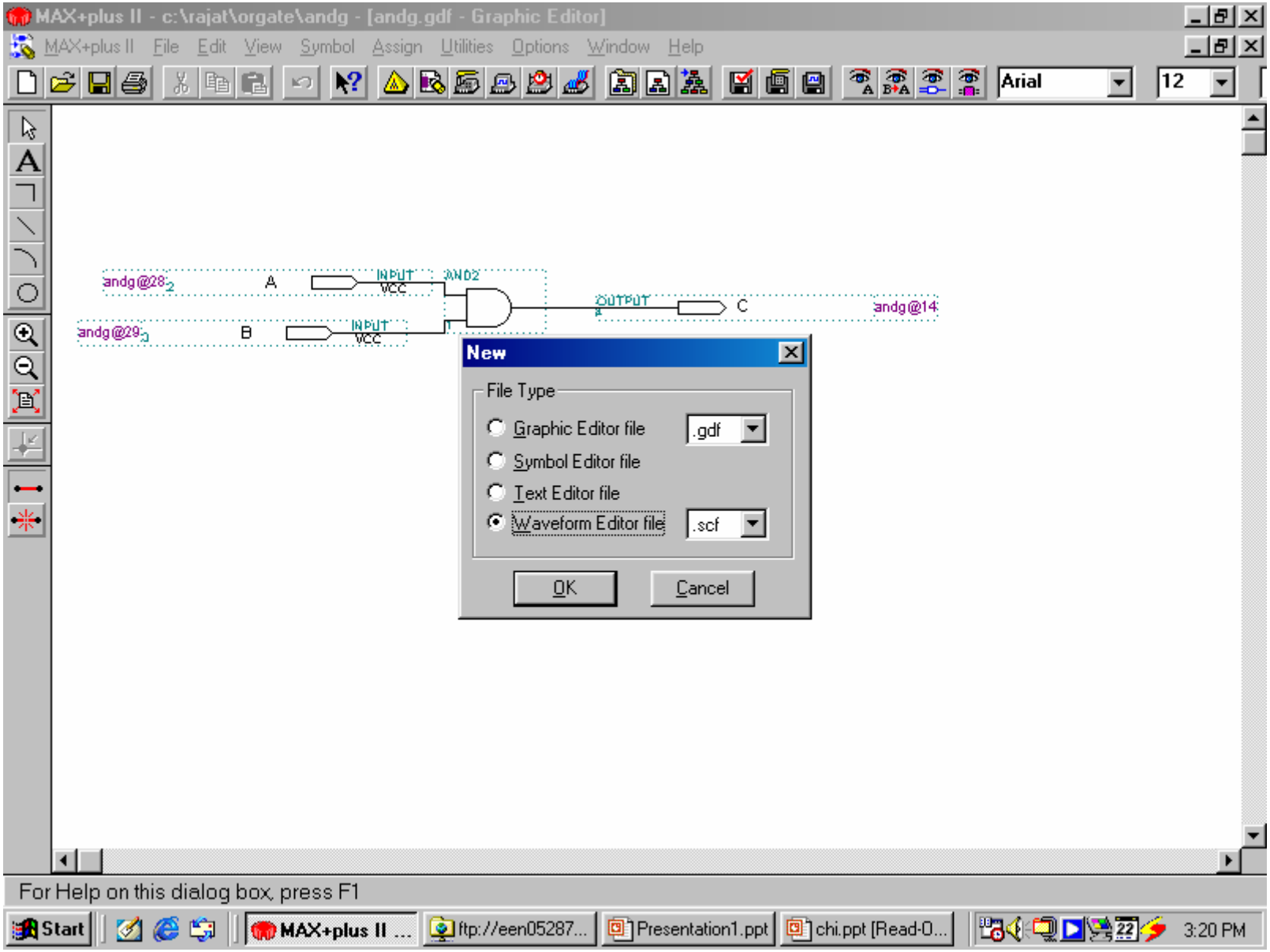
A. *Fitting the Design to a Component*

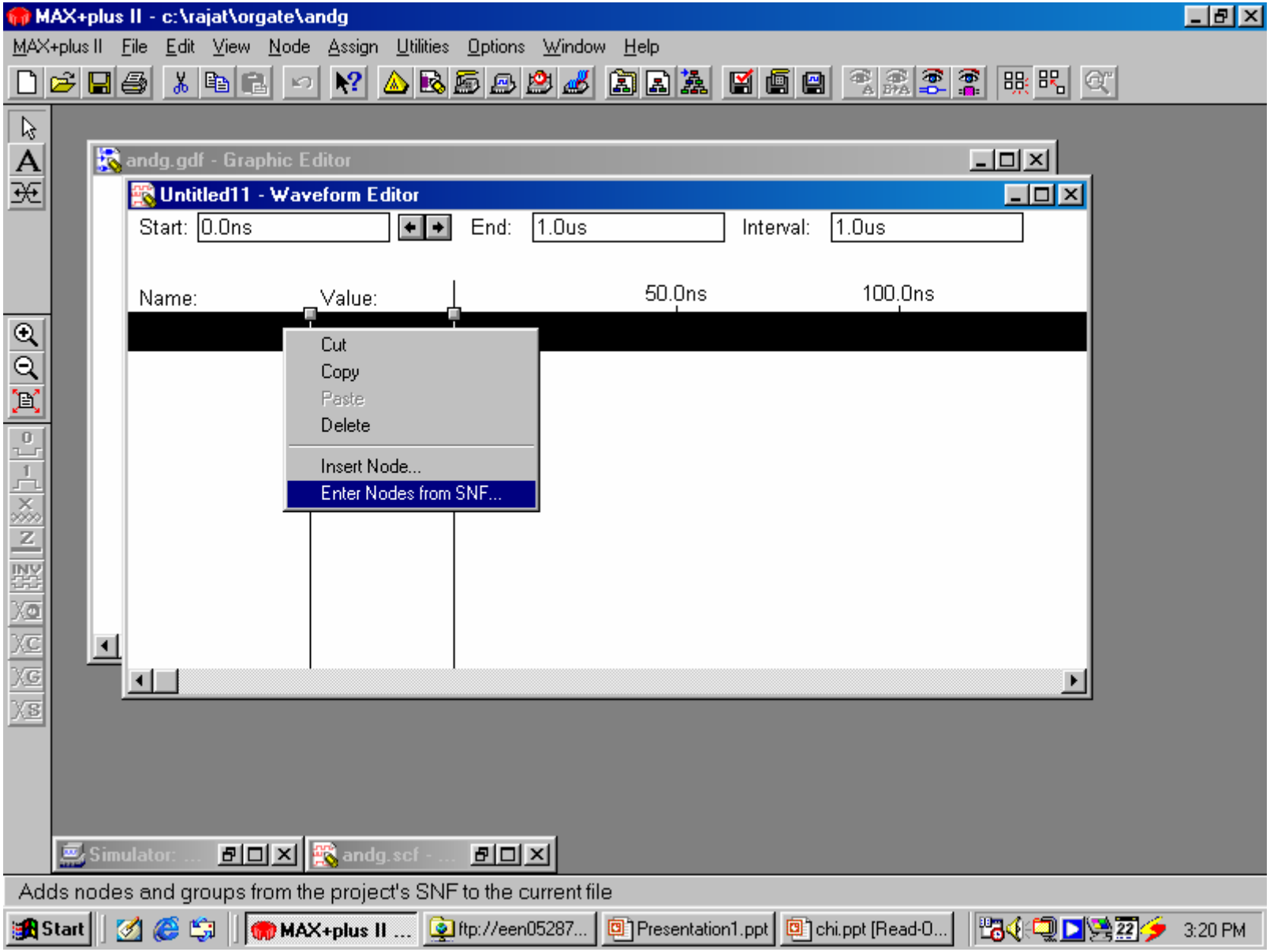

MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II
File
Edit
View
Symbol
Assign
Utilities
Options
Window
Help
Hierarchy Display
Graphic Editor
Symbol Editor
Text Editor
Waveform Editor
Floorplan Editor
Compiler
Simulator
Timing Analyzer
Programmer
Message Processor
Arial
12
A
INPUT
VCC
AND2
INPUT
VCC
OUTPUT
C
andg@14
Opens the Compiler window or brings it to the foreground
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:19 PM

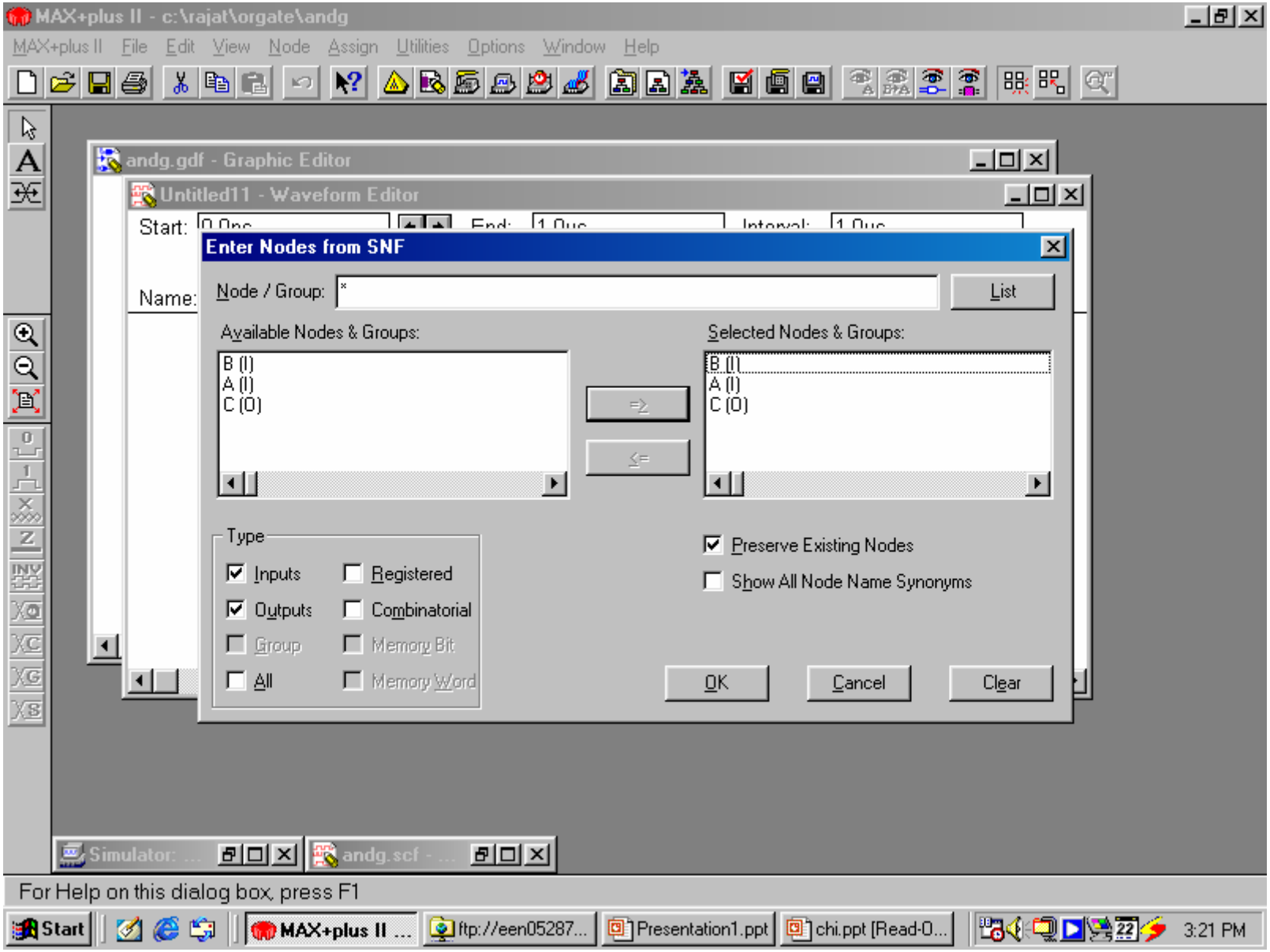

MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Processing Interfaces Assign Options Window Help
Compiler
Compiler Netlist Extractor
Database Builder
Logic Synthesizer
Partitioner
Fitter
Timing SNF Extractor
Assembler
0
50
100
Start
Stop
Simulator: ...
andg.scf - ...
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:19 PM

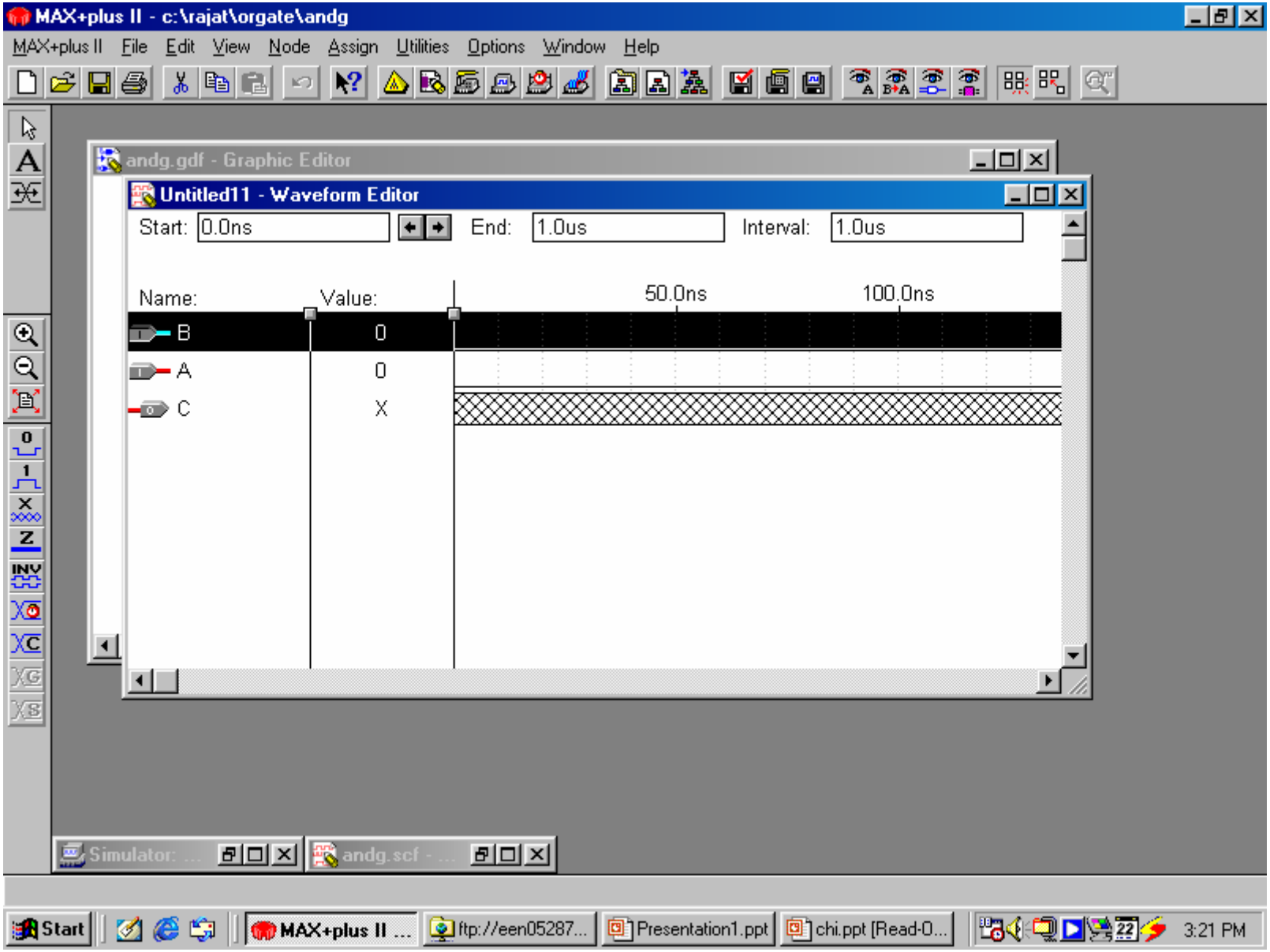
II. Circuit Simulation

B. *Creating a Waveform for use with the Simulator*


MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Arial
12
andg@28
A
INPUT
VCC
AND2
andg@29
B
INPUT
VCC
OUTPUT
C
andg@14
New
File Type
Graphic Editor file
.gdf
Symbol Editor file
Text Editor file
Waveform Editor file
.scf
OK
Cancel
For Help on this dialog box, press F1
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:20 PM

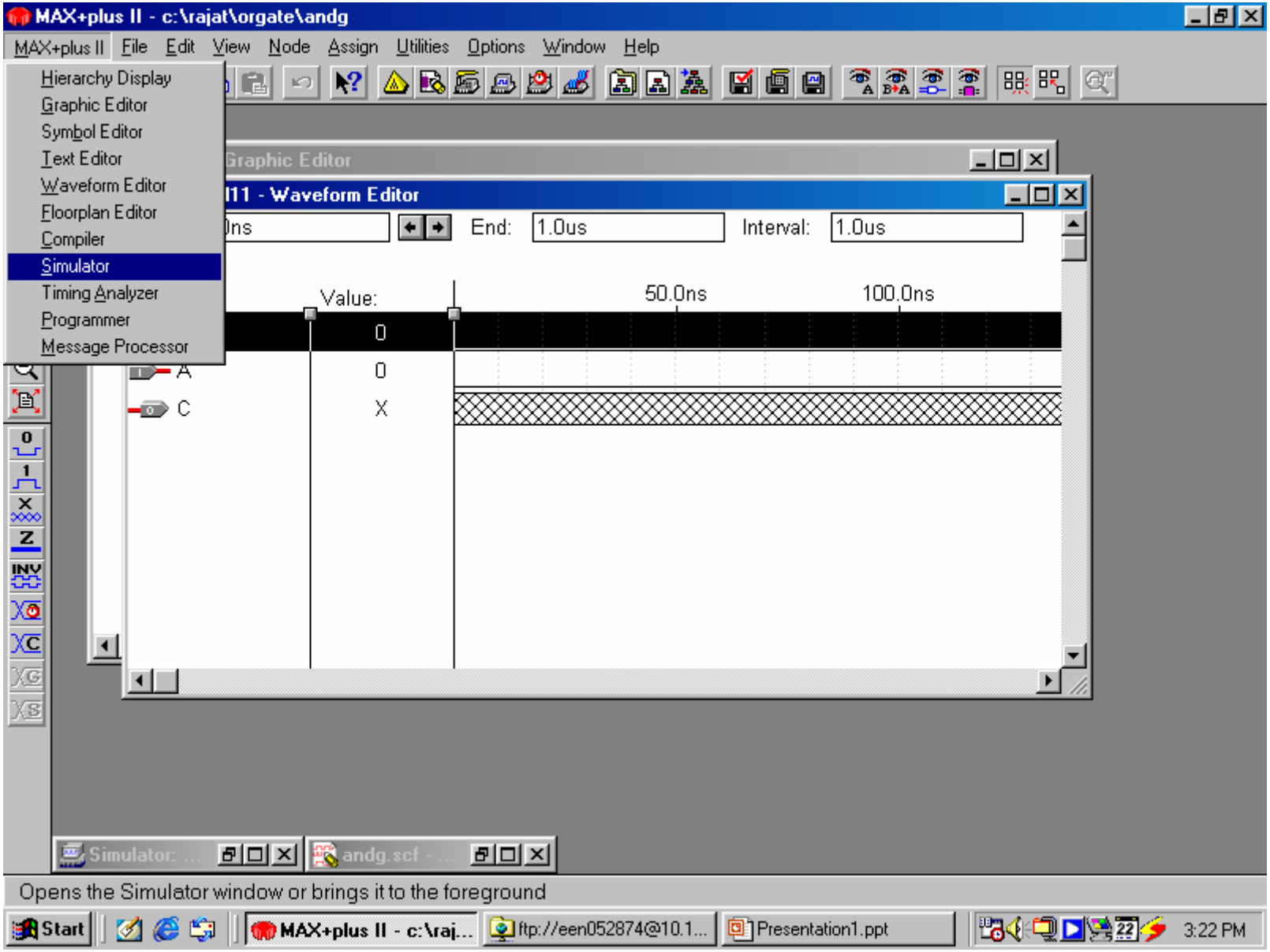

MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Edit View Node Assign Utilities Options Window Help
andg.gdf - Graphic Editor
Untitled11 - Waveform Editor
Start: 0.0ns
End: 1.0us
Interval: 1.0us
Name:
Value:
50.0ns
100.0ns
Cut
Copy
Paste
Delete
Insert Node...
Enter Nodes from SNF...
Simulator: ...
andg.scf - ...
Adds nodes and groups from the project's SNF to the current file
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:20 PM

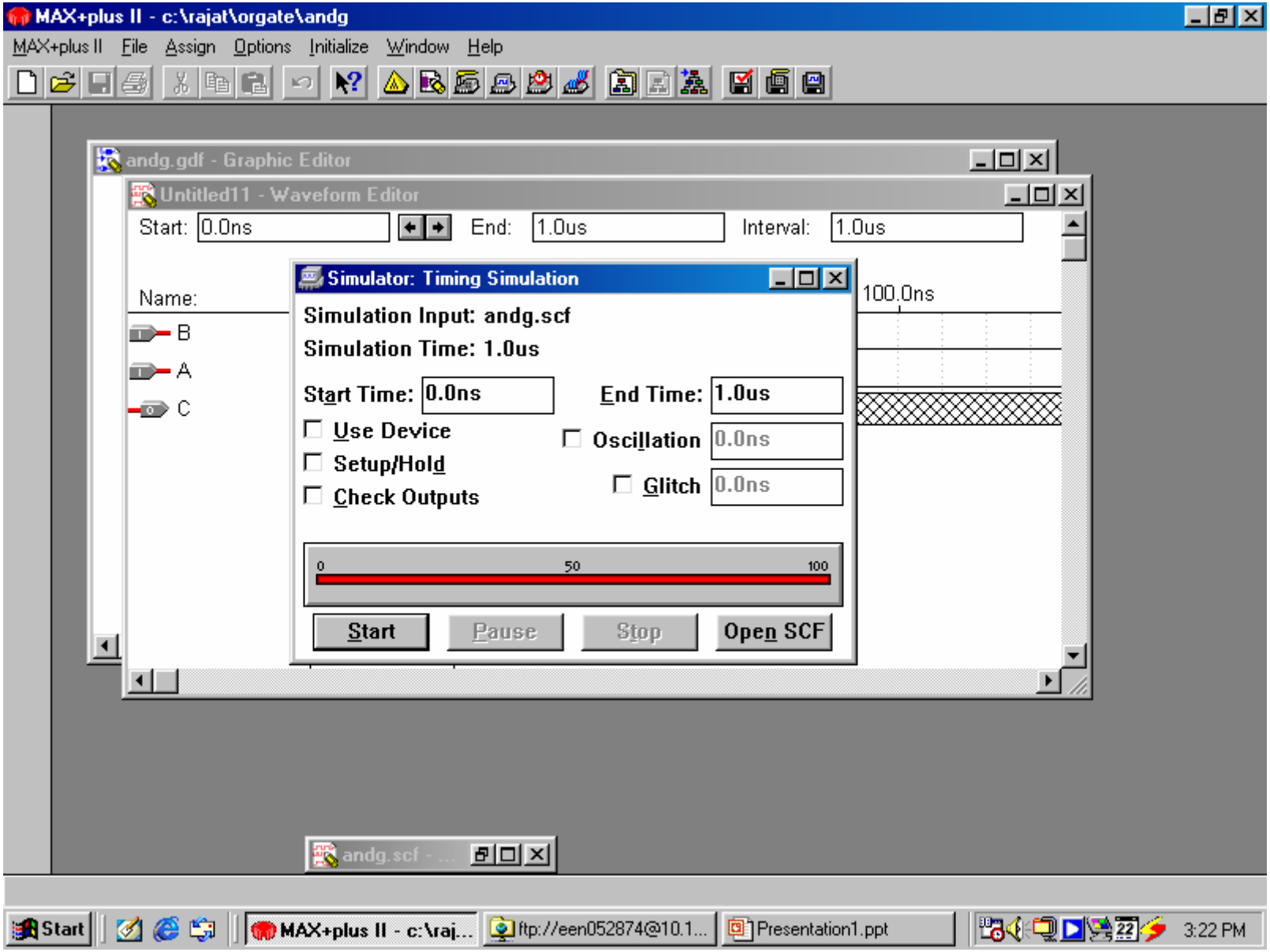

MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Edit View Node Assign Utilities Options Window Help
andg.gdf - Graphic Editor
Untitled11 - Waveform Editor
Start:
End:
Interval:
Name:
Enter Nodes from SNF
Node / Group: *
List
Available Nodes & Groups:
B (I)
A (I)
C (O)
Selected Nodes & Groups:
B (I)
A (I)
C (O)
=>
<=
Type
Inputs
Outputs
Group
All
Registered
Combinatorial
Memory Bit
Memory Word
Preserve Existing Nodes
Show All Node Name Synonyms
OK
Cancel
Clear
Simulator: ...
andg.scf - ...
For Help on this dialog box, press F1
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:21 PM

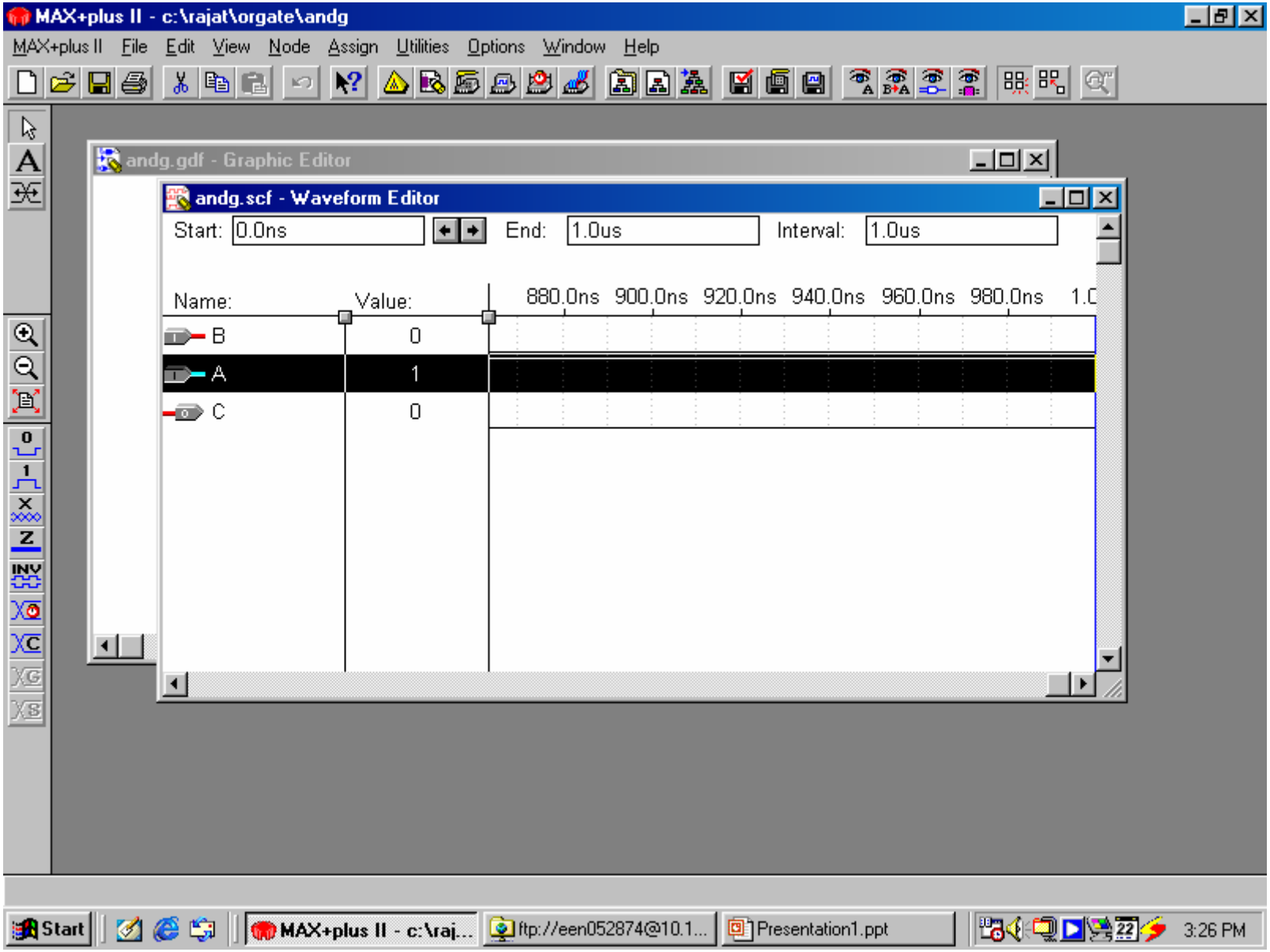

MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Edit View Node Assign Utilities Options Window Help
andg.gdf - Graphic Editor
Untitled11 - Waveform Editor
Start: 0.0ns
End: 1.0us
Interval: 1.0us
Name:
Value:
50.0ns
100.0ns
B 0
A 0
C X
Simulator: ...
andg.scf - ...
Start
MAX+plus II ...
ftp://een05287...
Presentation1.ppt
chi.ppt [Read-O...
3:21 PM

II. Circuit Simulation

C. Running the Simulator and Analyzing the Results

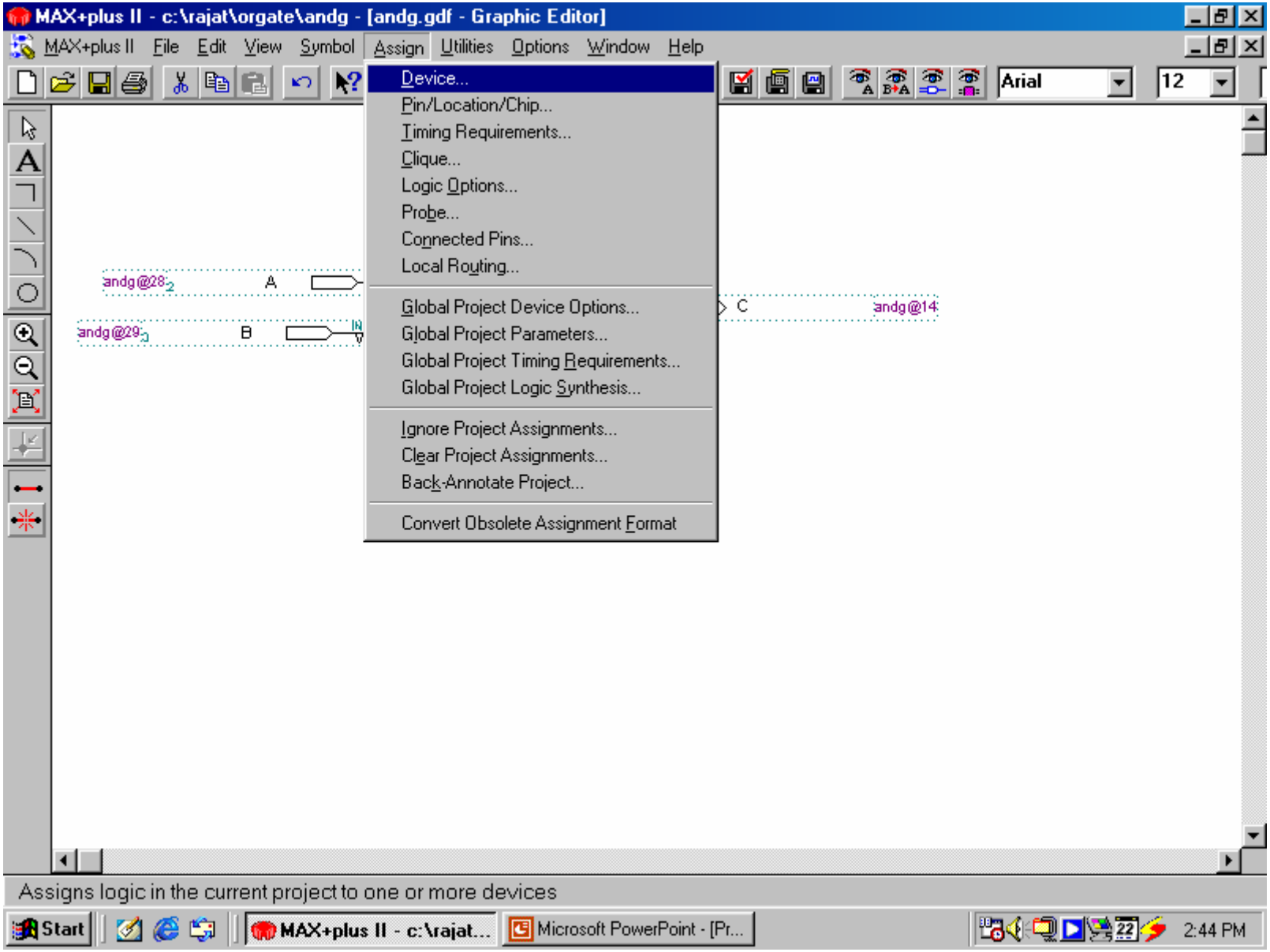

MAX+plus II - c:\rajat\orgate\andg
MAX+plus II
File
Edit
View
Node
Assign
Utilities
Options
Window
Help
Hierarchy Display
Graphic Editor
Symbol Editor
Text Editor
Waveform Editor
Floorplan Editor
Compiler
Simulator
Timing Analyzer
Programmer
Message Processor
Graphic Editor
11 - Waveform Editor
End:
1.0us
Interval:
1.0us
Value:
50.0ns
100.0ns
A
C
0
X
Simulator:
andg.scf -
Opens the Simulator window or brings it to the foreground
Start
MAX+plus II - c:\raj...
ftp://een052874@10.1...
Presentation1.ppt
3:22 PM

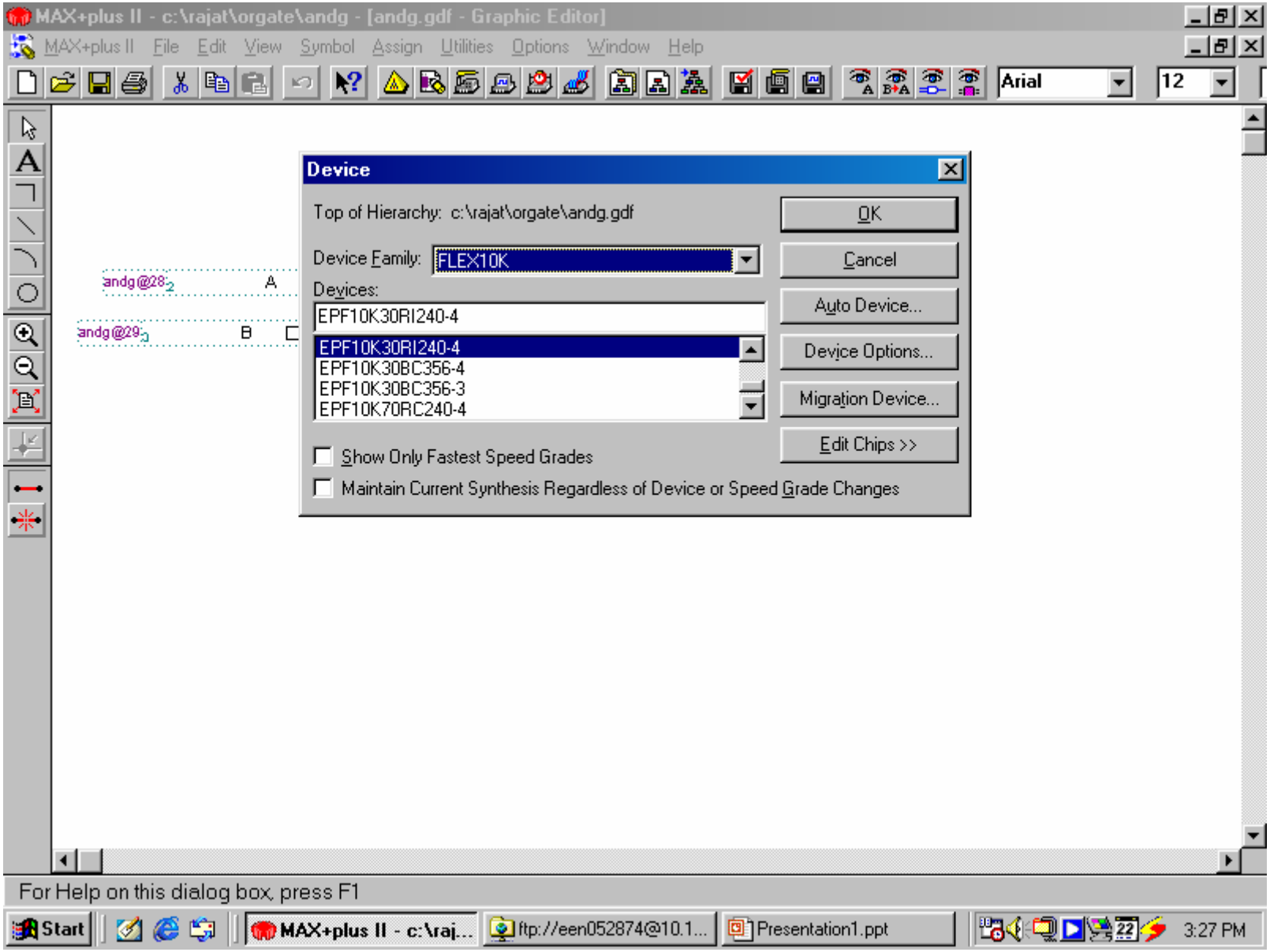

MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Assign Options Initialize Window Help
andg.gdf - Graphic Editor
Untitled11 - Waveform Editor
Start: 0.0ns
End: 1.0us
Interval: 1.0us
Name:
B
A
C
100.0ns
Simulator: Timing Simulation
Simulation Input: andg.scf
Simulation Time: 1.0us
Start Time: 0.0ns
End Time: 1.0us
Use Device
Setup/Hold
Check Outputs
Oscillation 0.0ns
Glitch 0.0ns
0
50
100
Start
Pause
Stop
Open SCF
andg.scf - ...
Start
MAX+plus II - c:\raj...
ftp://een052874@10.1...
Presentation1.ppt
3:22 PM


MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File Edit View Node Assign Utilities Options Window Help
andg.gdf - Graphic Editor
andg.scf - Waveform Editor
Start: 0.0ns
End: 1.0us
Interval: 1.0us
Name:
Value:
880.0ns 900.0ns 920.0ns 940.0ns 960.0ns 980.0ns
B 0
A 1
C 0
Start
MAX+plus II - c:\raj...
ftp://een052874@10.1...
Presentation1.ppt
3:26 PM

3.PROGRAMMING FPGA

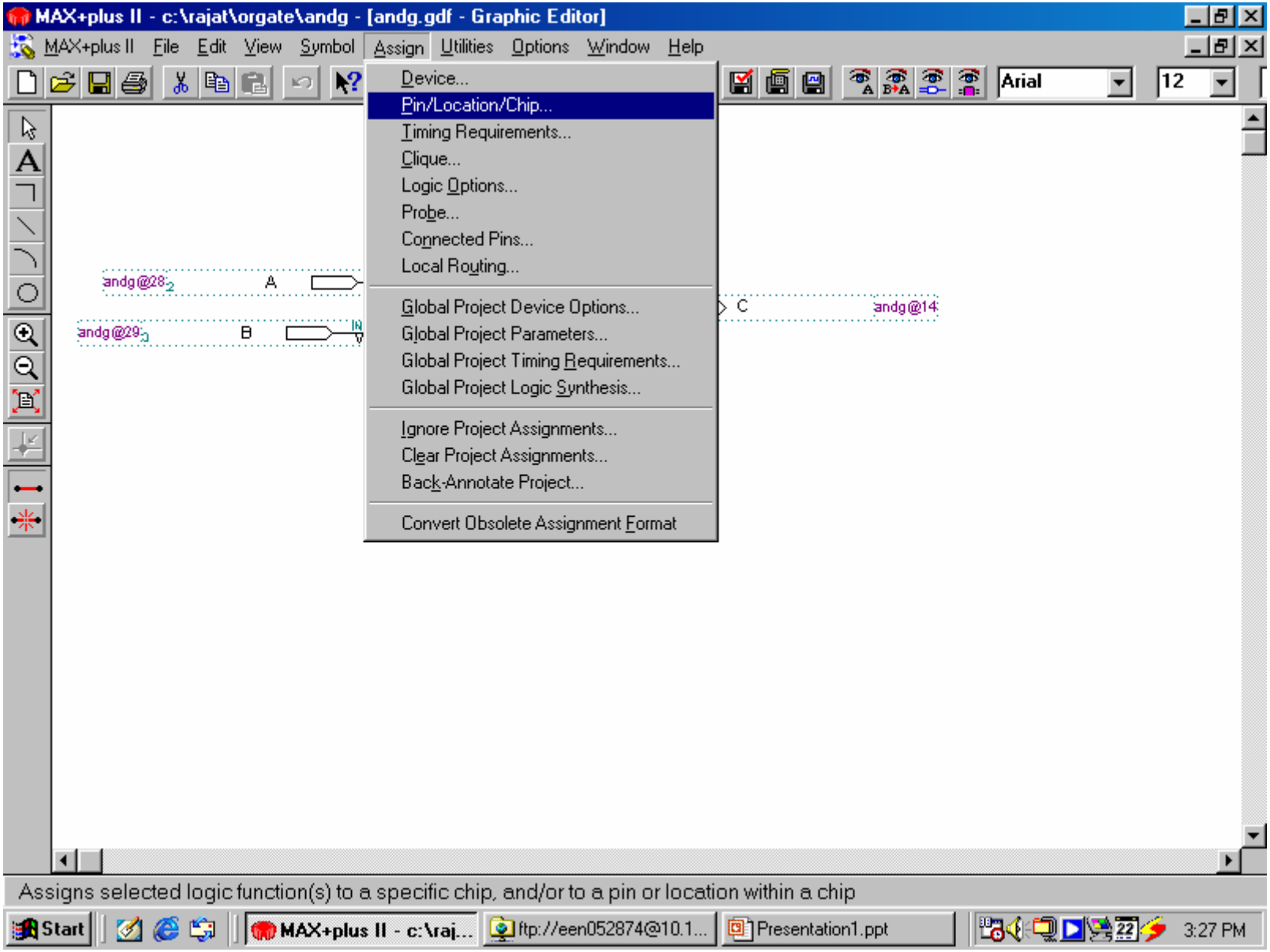
A.SELECTING THE CHIP

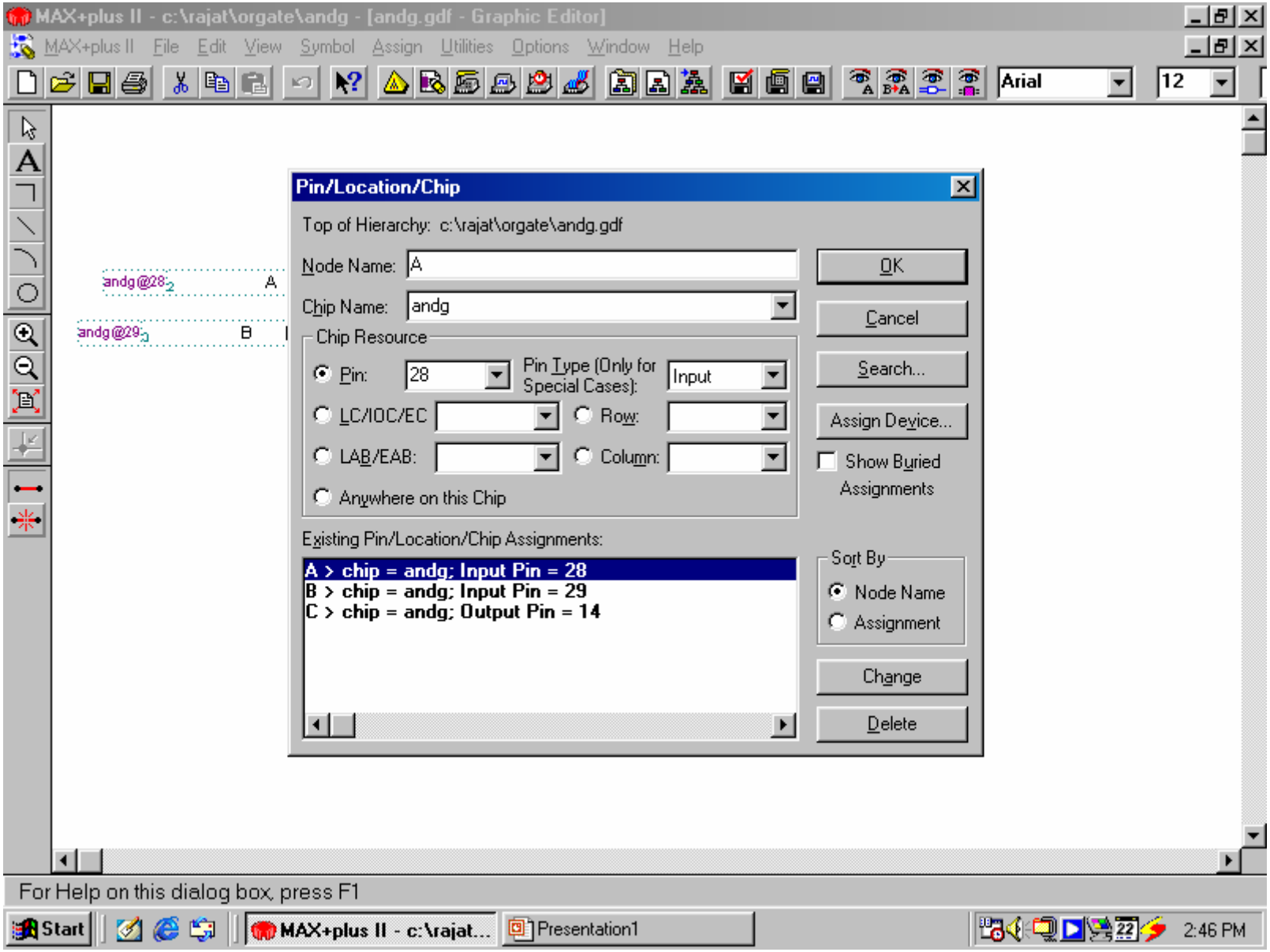

MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Device...
Pin/Location/Chip...
Timing Requirements...
Clique...
Logic Options...
Probe...
Connected Pins...
Local Routing...
Global Project Device Options...
Global Project Parameters...
Global Project Timing Requirements...
Global Project Logic Synthesis...
Ignore Project Assignments...
Clear Project Assignments...
Back-Annotate Project...
Convert Obsolete Assignment Format
Arial
12
andg@28
A
andg@29
B
C
andg@14
Assigns logic in the current project to one or more devices
Start
MAX+plus II - c:\rajat...
Microsoft PowerPoint - [Pr...
2:44 PM


MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Arial
12
Device
Top of Hierarchy: c:\rajat\orgate\andg.gdf
OK
Device Family: FLEX10K
Cancel
Devices:
EPF10K30RI240-4
Auto Device...
EPF10K30RI240-4
EPF10K30BC356-4
EPF10K30BC356-3
EPF10K70RC240-4
Device Options...
Migration Device...
Edit Chips >>
Show Only Fastest Speed Grades
Maintain Current Synthesis Regardless of Device or Speed Grade Changes
andg@28
A
andg@29
B
For Help on this dialog box, press F1
Start
MAX+plus II - c:\raj...
ftp://een052874@10.1...
Presentation1.ppt
3:27 PM

3.PROGRAMMING FPGA

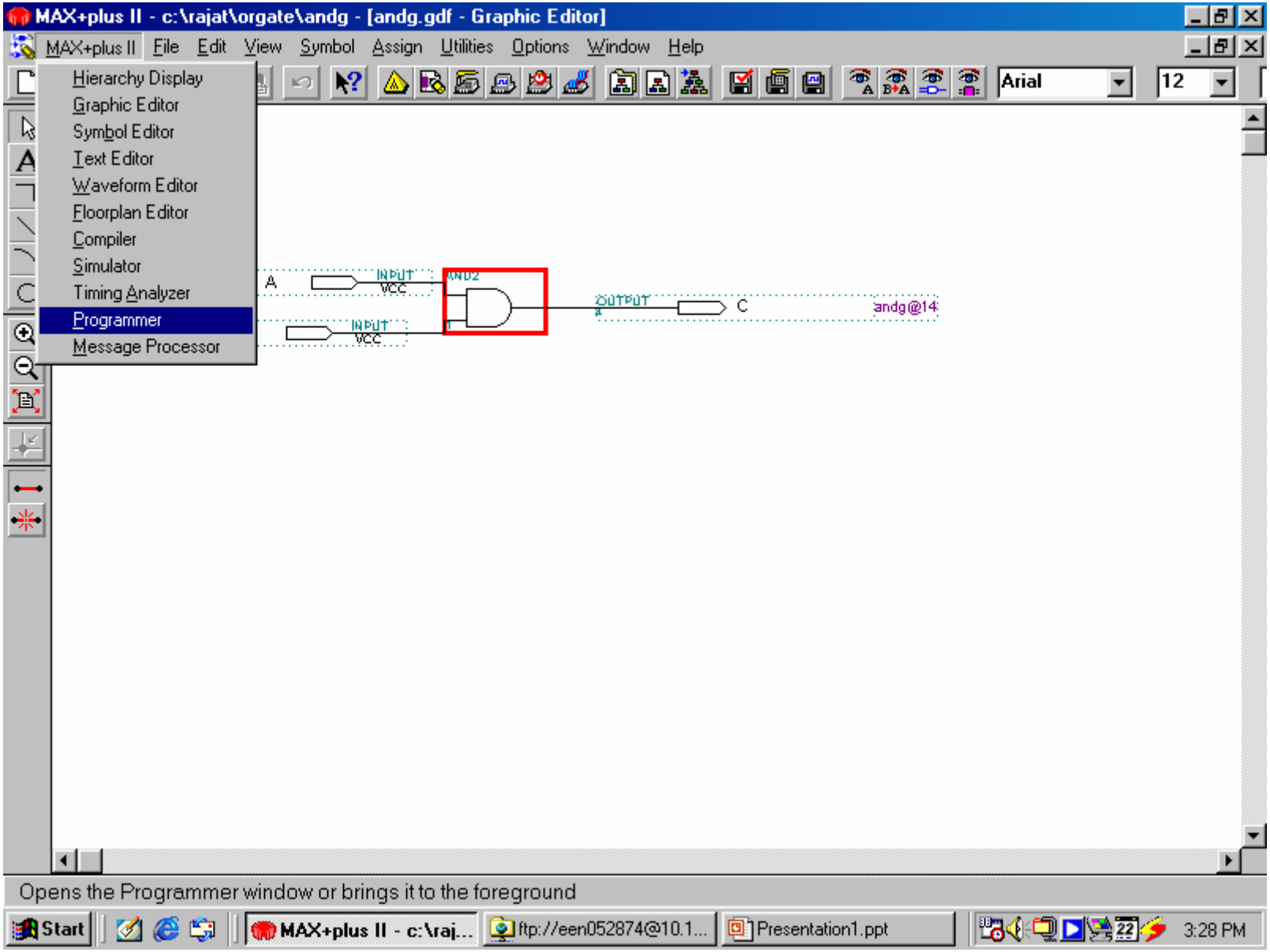
B.ASSIGNING PIN LOCATIONS

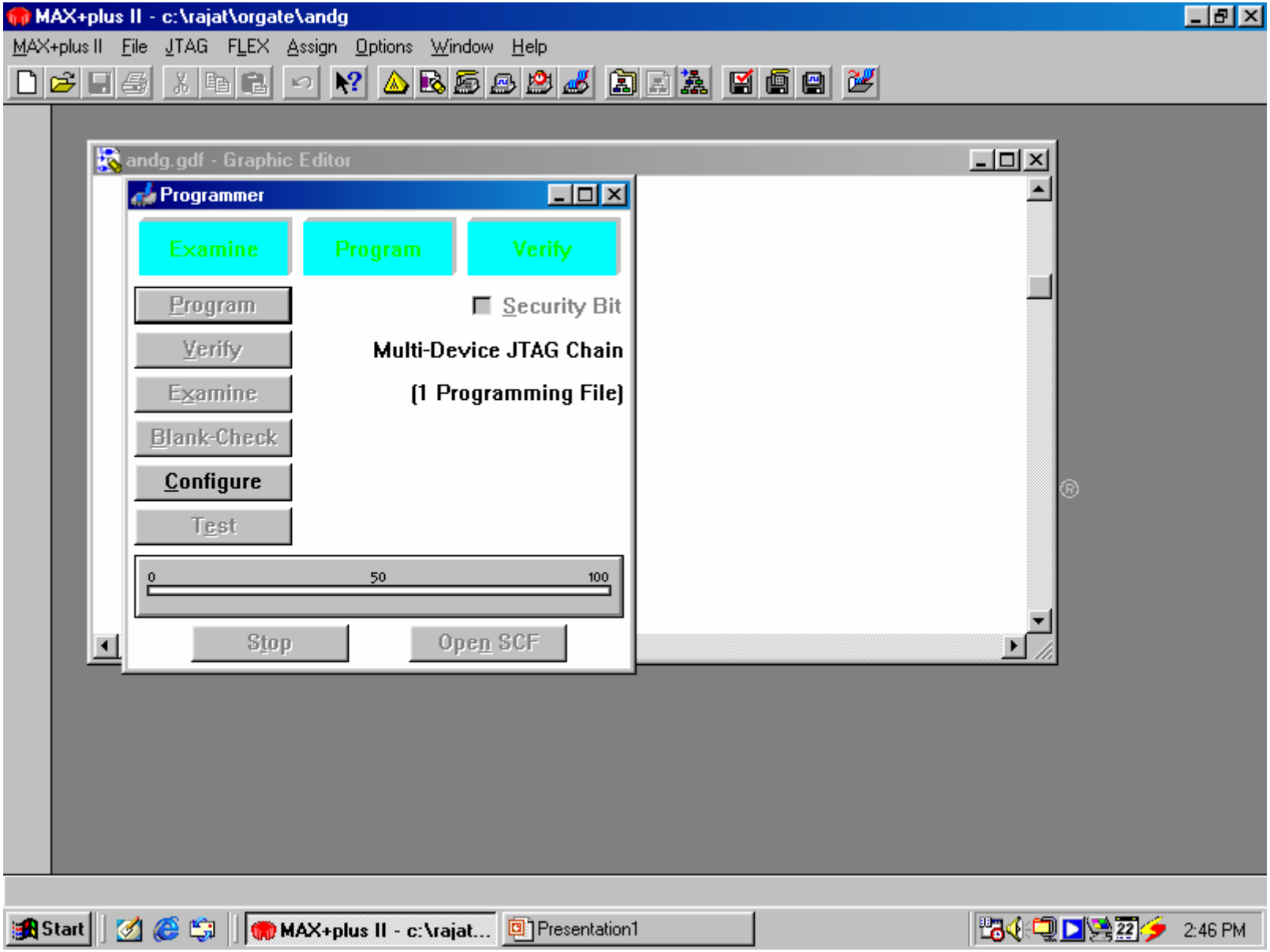

MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Device...
Pin/Location/Chip...
Timing Requirements...
Clique...
Logic Options...
Probe...
Connected Pins...
Local Routing...
Global Project Device Options...
Global Project Parameters...
Global Project Timing Requirements...
Global Project Logic Synthesis...
Ignore Project Assignments...
Clear Project Assignments...
Back-Annotate Project...
Convert Obsolete Assignment Format
Arial
12
andg@28
A
andg@29
B
C
andg@14
Assigns selected logic function(s) to a specific chip, and/or to a pin or location within a chip
Start
MAX+plus II - c:\raj...
ftp://een052874@10.1...
Presentation1.ppt
3:27 PM


MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II File Edit View Symbol Assign Utilities Options Window Help
Arial
12
andg@28
A
andg@29
B
Pin/Location/Chip
Top of Hierarchy: c:\rajat\orgate\andg.gdf
Node Name: A
Chip Name: andg
Chip Resource
Pin: 28
Pin Type (Only for Special Cases): Input
LC/IOC/EC
Row:
LAB/EAB:
Column:
Anywhere on this Chip
OK
Cancel
Search...
Assign Device...
Show Buried Assignments
Existing Pin/Location/Chip Assignments:
A > chip = andg; Input Pin = 28
B > chip = andg; Input Pin = 29
C > chip = andg; Output Pin = 14
Sort By
Node Name
Assignment
Change
Delete
For Help on this dialog box, press F1
Start
MAX+plus II - c:\rajat...
Presentation1
2:46 PM

3.PROGRAMMING FPGA

C.PROGRAMMING THE FPGA CHIP


MAX+plus II - c:\rajat\orgate\andg - [andg.gdf - Graphic Editor]
MAX+plus II
File
Edit
View
Symbol
Assign
Utilities
Options
Window
Help
Hierarchy Display
Graphic Editor
Symbol Editor
Text Editor
Waveform Editor
Floorplan Editor
Compiler
Simulator
Timing Analyzer
Programmer
Message Processor
Arial
12
A
INPUT
VCC
AND2
OUTPUT
C
andg@14
Opens the Programmer window or brings it to the foreground
Start
MAX+plus II - c:\raj...
ftp://een052874@10.1...
Presentation1.ppt
3:28 PM


MAX+plus II - c:\rajat\orgate\andg
MAX+plus II File JTAG FLEX Assign Options Window Help
andg.gdf - Graphic Editor
Programmer
Examine
Program
Verify
Program
Verify
Examine
Blank-Check
Configure
Test
Security Bit
Multi-Device JTAG Chain
(1 Programming File)
0
50
100
Stop
Open SCF
Start
MAX+plus II - c:\rajat...
Presentation1
2:46 PM